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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,853	07/31/2003	Han-Jong Kim	2557-000168/US	1965

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HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 8910
RESTON, VA 20195

EXAMINER	
WEINMAN, SEAN M	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 06/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,853	KIM, HAN-JONG	
	Examiner	Art Unit	
	Sean Weinman	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 31 July 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is responsive to the amendment filed on March 29, 2006. Claims 1-20 are pending.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1- 20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter that was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As per claim 1 and 7, in claim 1 "a high-speed control circuit for controlling high-speed operations of at least one of the processor core and the peripheral device in response to the selection signal" is not clearly understood. Additionally, in claim 1 "a low-speed control circuit for controlling low-speed operations of at least one of the processor core and the peripheral device in response to the selection signal" is not clearly understood. Paragraph [0032] of the specification recites, "In response to the selection signal SEL, the MUX 250 may electrically connect the high-speed control circuit 230 with the processor core 260 and the peripheral device 270, or may electrically connect the low-speed and low-power control circuit 240 with the processor core 260 and the peripheral device 270." Additionally, paragraph [0037] of the specification recites, "The selecting circuit 220 is capable of comparing the operating frequency

of the processor 200 with a predetermined threshold frequency. Based upon this comparison, the selecting circuit may output the selection signal SEL to the MUX 250." It is uncertain how the selection signal directly controls the high-speed control circuit and the low-speed control circuit in claim 1 and claim 7.

As per claim 10 and 20, "selecting a control circuit from a plurality of control circuits" in not clearly understood. For the reasons hereinabove it is unclear how the selection circuit directly selects a control circuit from a plurality of control circuits for controlling at least a first and a second device.

Any claim not specifically address above is being rejected as incorporating the deficiencies of a claim upon which it depends.

Claim Rejections – 35 USC § 103

The rejections are respectfully maintained and reproduced infra for Applicant's convenience.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 5-8, 10-11, 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (US Patent Application 2002/0026596) in view of Dai (US Patent Application 2002/0083356) and in further view of Applicant's Admission of Prior Art (AAPA).

As per claims 1 and 7, Kim teaches the invention comprising:

a selecting circuit for outputting a selection signal (Figure 2 Reference 140 and Paragraph [0017] lines 1-5);

a high-speed control circuit for controlling high-speed operations in response to the selection signal (Figure 2 Reference 130 and Paragraph [0014]); and

a low-speed and low-power control circuit for controlling low-speed and low-power operations in response to the selection signal (Figure 2 Reference 120 and Paragraph [0015]); and

a multiplexer for interfacing one of the high-speed control circuit and the low-speed and low-power control circuit (Figure 2 Reference 160 and Paragraph [0018]).

Kim, however, does not teach that the selecting circuit determines the operational state of the processor and outputs the selection signal based on the evaluation of the operational state of the processor. Additionally, Kim does not teach that the processor has a processor core and at least one peripheral device. Specifically, Kim teaches a processor with a high-speed control circuit and a low-speed control circuit, a multiplexer that is controlled by a selection signal for selecting either the high-speed or low-speed control circuits. Additionally, Kim teaches that a multiplexer is used to interface the high-speed or low-speed control circuit with the processor.

Dai teaches a processor control system that selects between two performance states, a high performance mode and a low power mode, and outputs a selection signal based on the determination of which operating state.

A selecting circuit for determining an operational state of the processor and for outputting a selection signal based on the evaluation (Paragraph [0013]). In summary, Dai teaches a selection circuit having two power states and determining which operating state is to be

implemented. Additionally, Dai teaches outputting a selection signal based on the determination of the operating state.

The AAPA teaches a processor having a processor core, peripheral device and a control circuit controlling the frequency of the processor core and the peripheral device.

A processor having a processor core and at least one peripheral device (Figure 1 Prior Art and Paragraphs [0006] and [0009])

It would have been obvious to one of ordinary skill in the art to combine the teachings of Kim, Dai, and Applicant's Admission of Prior Art (AAPA) because they all teach a processor having a controller unit to control the frequency of a processor. Dai AAPA teaches the deficiency of Kim by teaching a selection circuit for determining an operational state and outputting a selection signal based on that determination. Furthermore, the AAPA teaches the deficiency of Kim by teaching the processor having a processor core and at least one peripheral device.

As per claims 2 and 8,Kim teaches the invention comprising:

the high-speed control circuit controls the high-speed operations of one of at least the processor core and the peripheral device when the operational state determined is a normal mode (Figure 2 Reference 130 and Paragraph [0014]), and the low-speed and low-power control circuit controls the low-speed and low-power operations of one of at least the processor core and the peripheral device when the operational state determined is a slow mode (Figure 2 Reference 120 and Paragraph [0015]). The AAPA teaches the processor having a processor core, peripheral device and a control circuit controlling the frequency of the processor core and the peripheral device.

As per claim 5, the AAPA teaches the invention comprising:

processor core is a central processing unit (CPU) (Figure 1 Prior Art and Paragraphs [0006])

As per claim 6, The AAPA teaches the invention comprising:

the peripheral device is at least one of a wireless LAN card, a PC card, and a liquid crystal display (LCD) (Figure 1 Prior Art and Paragraphs [0009]).

As per claim 10, Kim teaches the invention comprising:

selecting a control circuit from a plurality of control circuits, the control circuit for controlling one of at least a first device and a second device (Figure 2 Reference 140 and Paragraph [0017]).

As per claim 11, Kim teaches the invention comprising:

an interface device for interfacing the selected control circuit with at least one of the first device and the second device (Figure 2 Reference 160 and Paragraph [0018]).

As per claim 15, 16, and 17 Dai teaches the invention comprising:

the circuit for selecting evaluates a mode of the processor in a process of selecting the control circuit from the plurality of control circuits (Abstract lines 1-5 and Paragraphs [0013]).

As per claim 18, Kim teaches the invention comprising:

control circuits includes at least a high-speed control circuit and a low-speed and low-power control circuit (Figure 2 Reference 130 and 120 and Paragraph [0014] and [0015]);

As per claim 19, the AAPA teaches the invention comprising:

first device is a processor core and the second device is a peripheral device (Figure 1 Prior Art and Paragraphs [0006] and [0009]).

As per claim 20, it is directed at the method of controlling a first device and a second device with a selected control circuit. Since Kim teaches a processor comprising a circuit of controlling a first device and a second device with a selected control circuit, Kim teaches the method of controlling a first device and a second device with a selected control circuit.

Response to Arguments

Applicant's remarks filed on March 29, 2006 have been fully considered but are not persuasive.

In the remarks, Applicant argues that in the substance of Kim that the second clock generator does not receive any selection signal from the first clock control and/or the clock selection unit. The examiner respectfully disagrees with Applicant's position. Paragraph [0032] of the specification recites, "In response to the selection signal SEL, the MUX 250 may electrically connect the high-speed control circuit 230 with the processor core 260 and the peripheral device 270, or may electrically connect the low-speed and low-power control circuit 240 with the processor core 260 and the peripheral device 270." Additionally, paragraph [0037] of the specification recites, "The selecting circuit 220 is capable of comparing the operating frequency of the processor 200 with a predetermined threshold frequency. Applicant does not teach that either the high-speed or low-speed control circuits receive the selection signal. Applicant teaches that the selection signal is received by the multiplexer and the multiplexer electronically connects the control circuits to the processor core and the peripheral device.

Additionally in the remarks, Applicant argues "a clock generator is not necessarily a control circuit". The examiner respectfully disagrees with Applicant's position. Paragraph [0034]

of the specification recites, "The high-speed control circuit 230 and the low-speed and low-power control circuit 240, respectively, may divide an input clock signal (not shown) and include a circuit (not shown) used to output the divided input clock signal." As stated in the rejection and the reasons stated above clock generators can be considered control signals.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sean Weinman whose phone number is (571) 272-2744. The examiner can normally be reached on Monday-Friday from 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667. The fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sean Weinman
Examiner
Art Unit 2115

CHUN CAO
PRIMARY EXAMINER